

Generation and Circuitry Implementation of N -double Scroll Delayed Chaotic Attractors

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Abstract—A first-order delayed chaotic model with n -double scroll attractors is investigated. The associated piecewise-linear activation function requires only a few operational amplifiers, which can easily be realized by an electronic circuit. The typical waveforms and phase portraits are plotted to illustrate n -double scroll chaotic oscillations.

Keywords—delay; chaotic attractor; n -double scroll; circuitry implementation; chaotic oscillation

I. INTRODUCTION

The theoretical study and circuitry implementation of more complex chaotic systems have been a key issue in various technological and engineering applications. Indeed, there were reported many multi-scroll, n -double scroll oscillators, which are produced with ODEs [1-2], where the activation function assumes a sine function, a piecewise linear function, or a hysteresis series, etc. Due to additional breakpoints owned by such activation functions, these systems exhibit hyperchaotic oscillations with multiple positive Lyapunov exponents.

On the other hand, chaotic behaviors have been found in various simple first-order systems with delayed feedback. This implies the evolution of state of such a system inherently depends on its history as well as its present state [3]. A diversity of delayed systems stemming from biology, ecology and engineering can be considered as models to analyze and implement hyperchaos [4-8].

In this pursuit, we study a novel delayed chaotic model capable of generating n -double scroll chaotic oscillations, where the nonlinear activation function is mathematically a PWL function and its circuitry implementation requires only several operational amplifiers. Experimental results show that the proposed attractor can exhibit mono-scroll, one- two-, three- or four-double scroll chaotic oscillations by adjusting the value of a single parameter.

The rest of this paper is organized as follows. In Section 2, the mathematical model of the proposed n -double scroll system is described. In Section 3, the electronic circuitry implementation of this system is discussed and analyzed in detail. Finally, some concluding remarks are given in Section 4.

II. MATHEMATICAL MODEL

In this paper, we propose an n -double scroll delayed chaotic model:

$$\frac{dx}{dt} = -x(t) + g[x(t - \tau)] \quad (1)$$

where τ is a delay time, g is a piecewise-linear activation function of the form:

$$g_{2n}(x) = m_n x + \frac{1}{2} \sum_{i=1}^n (m_{i-1} - m_i) (|x + c_i| - |x - c_i|) \quad (2)$$

n denotes number of double scrolls, m_i ($i = 1, \dots, n$) and c_i ($i = 1, \dots, n$) represent the slopes and values in the abscissa corresponding inflexions of the piecewise-linear activation function, respectively. As an example, when $n = 4$, $m_0 = m_2 = m_4 = -6.5$, $m_1 = m_3 = -8.5$, $c_1 = 0.8$, $c_2 = 2.4$, $c_3 = 4$, $c_4 = 5.6$, $\tau = 10$, the activation function is shown in Fig. 1, and the system (1) shows a four-double scroll chaotic oscillations, plotted in Fig. 2.

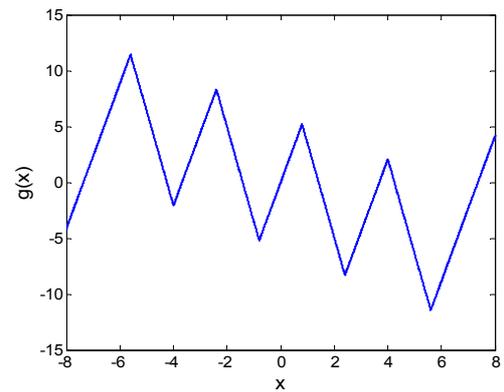


Fig. 1. Waveform diagram of a piecewise-linear function.

III. CIRCUITRY IMPLEMENTATION

In this section, an electronic circuit is designed to realize an n -double scroll delayed system. The circuit consists of a

piecewise-linear activation function circuit unit, a time delay circuit unit, an integration circuit unit and a low-pass filter. Common resistors, capacitors, inductances and operational amplifiers are employed to realize these circuit units. DC voltage sources supply energy of the circuit system.

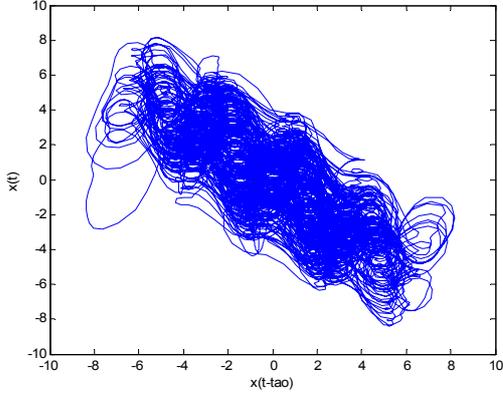


Fig. 2. Phase trajectories of the *four-double scroll* chaotic attractor.

A. Circuit Implementation of the Piecewise-linear Activation Function

To facilitate the circuitry design, piecewise-linear activation function (6) for four-double scroll oscillator is reformulated as follows:

$$\begin{aligned}
 g_8(x) = & m_4x + \frac{1}{2}(m_0 - m_1)(|x + c_1| - |x - c_1|) \\
 & + \frac{1}{2}(m_1 - m_2)(|x + c_2| - |x - c_2|) \\
 & + \frac{1}{2}(m_2 - m_3)(|x + c_3| - |x - c_3|) \\
 & + \frac{1}{2}(m_3 - m_4)(|x + c_4| - |x - c_4|)
 \end{aligned} \quad (3)$$

Obviously, the waveform diagram of the piecewise-linear function (3) can easily be varied by adjusting the values of m_i and c_i , $i = 1, \dots, n$. Let

$$\begin{cases} m_0 = m_2 = m_4 = ka \\ m_1 = m_3 = kb \end{cases} \quad (4)$$

where $k > 0$ is a common scaling factor of all the slopes, $a > 0$ and $b < 0$ are initial slopes of the line segments involved in the function (3). Hence, we can adjust all slopes synchronously by changing the value of k .

The function (3) can be circuitry implemented by a combination of six operational amplifiers and assistant circuits, as shown in Fig. 3.

The operational amplifiers ($\mu A741$ U_1-U_6) are employed to realize the gain control, subtraction and reversion operations.

The values of the resistors are: $R_1 = R_3 = R_5 = R_7 = R_{15} = R_{16} = 1k\Omega$, $R_2 = R_4 = R_6 = R_8 = 15k\Omega$, $R_9 = R_{10} = R_{11} = R_{12} = 2k\Omega$, $R_{13} = 307\Omega$, $R_{14} = 2k\Omega$. The constant voltage sources are: $V_1 = 1.4V$, $V_2 = -1.4V$, $V_3 = 4.2V$, $V_4 = -4.2V$. The voltages of the electronic sources are $\pm 12V$. All of the slopes in (3) are changed synchronously by adjusting the value of resistor R_{14} .

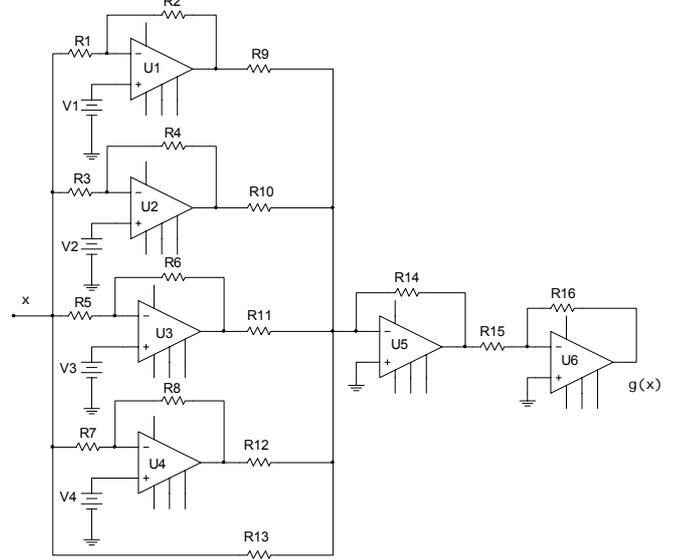


Fig. 3. A circuitry implementation of $g_8(x)$.

The DC sweep analysis result of the piecewise-linear activation function circuit unit is given in Fig. 4.

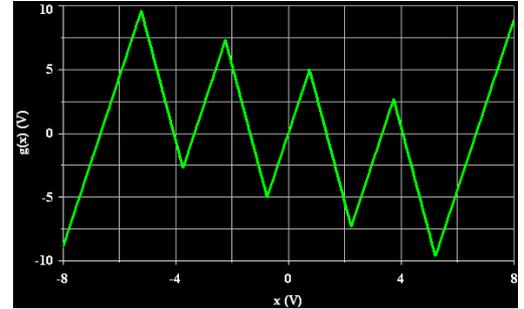


Fig. 4. The DC sweep analysis result of the piecewise-linear function circuit.

B. Circuit Implementation of the Time Delay Unit

A circuit implementation for the delay unit is plotted in Fig. 5. This is a network of T -type LCL filters with matching resistors at the input and the output. The time delay can be approximated by

$$T_{Delay} = n\sqrt{2LC}, \quad n \geq 1, \quad (5)$$

where n is the number of the LCL filter. From (5), it can be seen that the value of the time delay can be tuned by changing the values of the inductances and capacitors in circuit unit, or changing the number of the LCL filter. Notably, the time delay unit will somewhat bring a little attenuation of the circuit gain. To eliminate this hurdle, two additional operational amplifiers

(U_7 and U_8) are used to adjust the circuit gain. Inductances $L_i = 9.5mH$ ($i = 1, 2, \dots, 20$), capacitors $C_i = 525 nF$ ($i = 1, 2, \dots, 10$) and resistors $R_{17} = R_{18} = R_{21} = 10k\Omega$, $R_{19} = R_{20} = 1k\Omega$, $R_{22} = 30k\Omega$ are chosen, respectively. The effectiveness of the time delay unit is demonstrated by observing the output of the circuit unit when a sine wave with frequency $1kHz$ and amplitude $1.35V$ is given, as shown in Fig. 6.

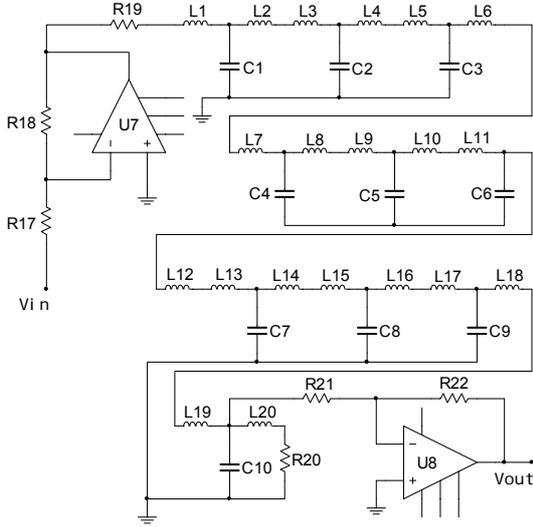


Fig. 5. Circuit implementation of the time delay unit.

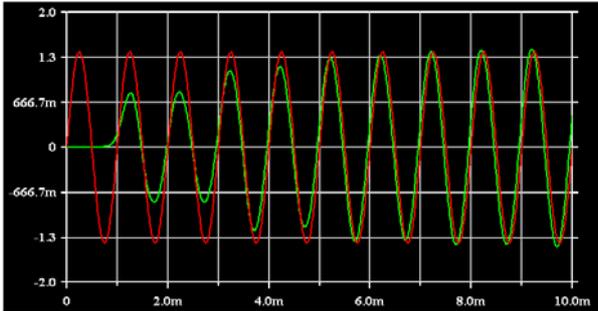


Fig. 6. Input (red waveform) and output (green waveform) of the proposed time delay unit when a sine wave is given.

C. Circuit Implementation of the N -double Scroll Delayed Chaotic Model

Now, the proposed n -double scroll chaotic system can be implemented by a piecewise-linear activation function circuit unit, a time delay circuit unit, an integration circuit unit and a low-pass filter ($R_0 C_0$), as shown in Fig. 7. For simplification, we use block diagrams to replace those already designed circuit units.

The dimensionless delay parameter τ is calculated according to the rule

$$\tau = T_{Delay} / R_0 C_0 \quad (6)$$

A standard node analysis of the circuit shows that the state equation that governs the dynamical behavior of the circuit is

$$\frac{dx(t)}{dt} = -\frac{1}{R_{24}C_{11}}x(t) + \frac{1}{R_{23}C_{11}}g[x(t-\tau)] \quad (7)$$

when $R_{23} = R_{24} = 10k\Omega$, $R_0 = 1k\Omega$, $C_{11} = 10nF$, $C_0 = 100nF$, Eq. (6) is equivalent to system (1) with activation function (3) and $\tau = 10$. In addition, the coefficients of $x(t)$ and $g[x(t-\tau)]$ can be varied independently by adjusting the values of resistors R_{24} and R_{23} .

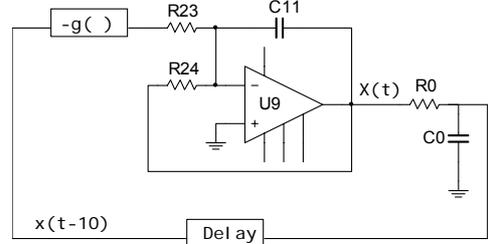
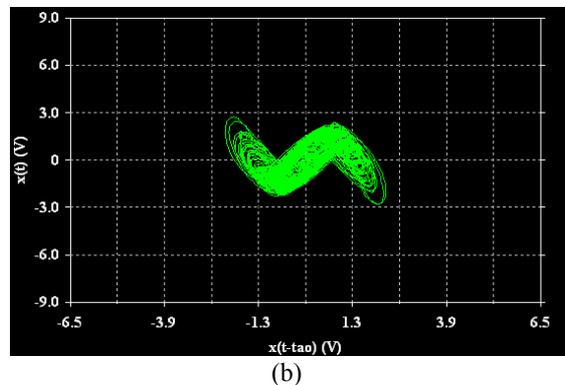
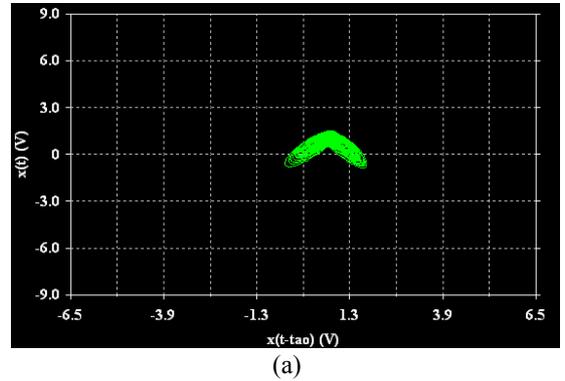
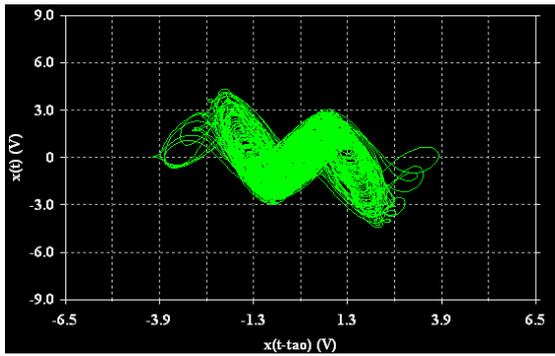


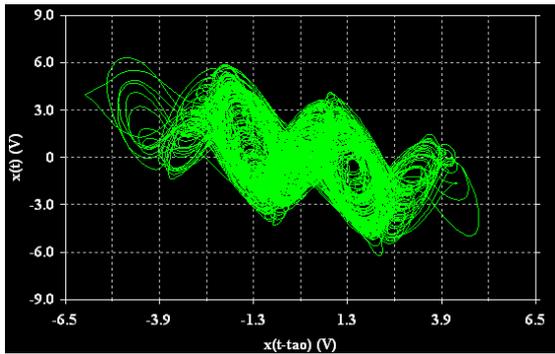
Fig. 7. Circuit implementation of the n -double scroll chaotic model.

Through experimental observation, we find that the proposed n -double scroll circuit can exhibit mono-, two- or three-double-scroll chaotic oscillations with the change of the value of resistor R_{14} . The respective phase plane diagrams of the chaotic double scroll circuits are given in Fig. 8. A comparison between Fig. 2 and Fig. 8 (e) indicates a qualitative agreement between the numerical simulation and the experimental measurement.

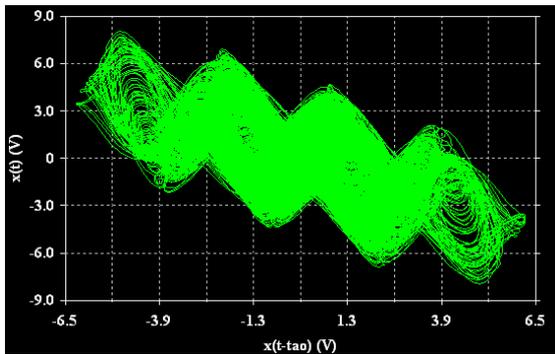




(c)



(d)



(e)

Fig. 8. Phase portraits of the n -double scroll chaos generator: (a) a mono-scroll oscillation when $R_{14} = 620\Omega$; (b) a one-double scroll oscillation when $R_{14} = 1.0k\Omega$; (c) a two-double scroll oscillation when $R_{14} = 1.3k\Omega$; (d) a three-double scroll oscillation when $R_{14} = 1.8k\Omega$; (e) a four-double scroll oscillation when $R_{14} = 2.0k\Omega$.

IV. CONCLUSION

We have presented a first-order delayed model with PWL activation function that displays double scrolls chaotic behavior, and have proposed a scheme for its circuit implementation. By adjusting the value of a single resistor, this simple circuit exhibits complex chaotic behaviors such as (a) a mono-scroll chaotic oscillation and (b) one-, two-, three- or four-double scroll chaotic oscillations.

The proposed chaotic circuit may be used as a delayed multi-scroll chaos generator, a chaotic neuron circuit unit, or

even a cell for delayed cellular neural network. It has potential applications to secure communication and signal processing.

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